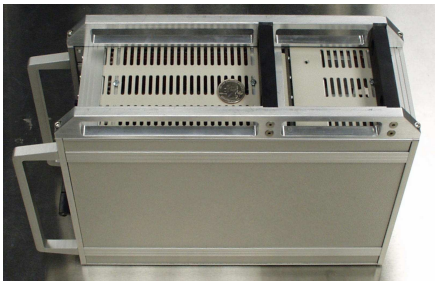
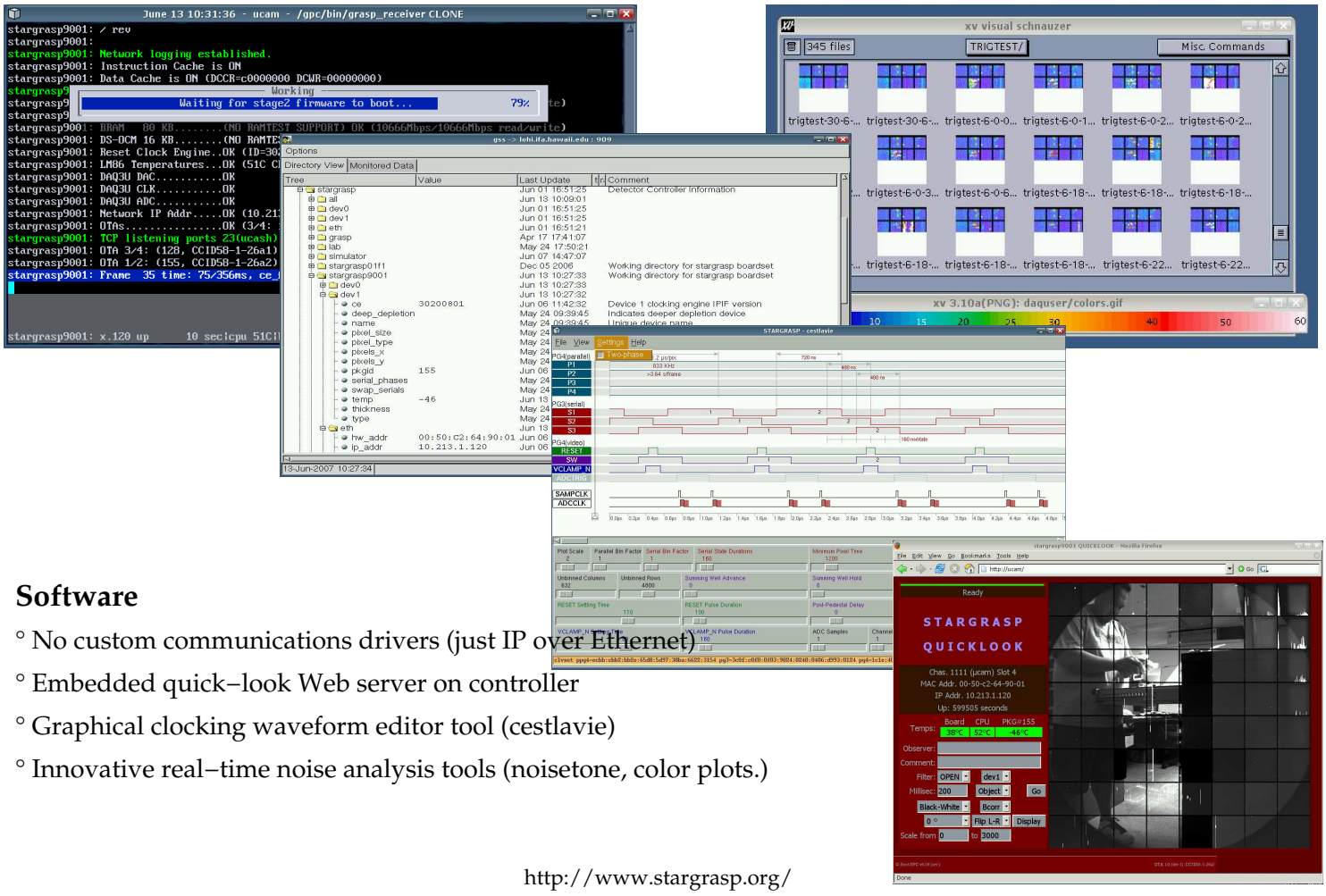
June 8, 2007 STARGRASP Info–Sheet

° 64 channels per chassis
° 2 "clocking engines" per boardset (8 per chassis)
° 2.4 Mpixels/second possible on each channel
° 16 bit analog to digital converters (ADCs)
° High speed (up to 10 MSPS) multi–sampling and/or multi–gain techniques are possible
° On–board DDR (laptop SoDIMM memory)
° On–board embedded PowerPC processors
° >2.4 Gbits/second fiber bandwidth per chassis (>600 Mbits of actual pixel data per boardset)



STARGRASP Controller Chassis

° 5 e– RMS read noise achieved on E2V CCID44–82
° 6 e– RMS read noise achieved on CCID58 OTA CCD



Software

° No custom communications drivers (just IP over Ethernet)
° Embedded quick–look Web server on controller
° Graphical clocking waveform editor tool (cestlavie)
° Innovative real–time noise analysis tools (noisetone, color plots.)