IOTA: the array controller for a gigapixel OTCCD camera for Pan-STARRS

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ABSTRACT

The PanSTARRS project has undertaken an ambitious effort to develop a completely new array controller architecture that is fundamentally driven by the large 1gigapixel, low noise, high speed OTCCD mosaic requirements as well as the size, power and weight restrictions of the PanSTARRS telescope. The result is a very small form factor next generation controller scalar building block with 1 Gigabit Ethernet interfaces that will be assembled into a system that will readout 512 outputs at ~1 Megapixel sample rates on each output. The paper will also discuss critical technology and fabrication techniques such as greater than 1MHz analog to digital converters (ADCs), multiple fast sampling and digital calculation of multiple correlated samples (DMCS), ball grid array (BGA) packaged circuits, LINUX running on embedded field programmable gate arrays (FPGAs) with hard core microprocessors for the prototype currently being developed.

Keywords: Digital multiple correlated sampling, Analog to Digital Converter, array controller, FPGA, LINUX.

INTRODUCTION

The requirements imposed on the array controller for the PanSTARRS Orthogonal Transfer Array (OTA) in an 8x8 mosaic presents a formidable challenge to any existing design. Despite the presence of an ongoing array controller development program at the Institute for Astronomy, a completely new effort was undertaken to produce a next generation design that could scale up to the needs of a gigapixel focal plane instrument. The team that was assembled to produce this design consisted of 2 scientists, 3 hardware/firmware engineers and 2 software engineers each with specific expertise and experience in critical areas.

DEVELOPMENT AND INFRASTRUCTURE PLAN

A multiphase plan has been developed to produce the IOTA array controller. A distinct infrastructure and prototype phase was identified as critical for success and the Institute for Astronomy has acquired new CAD development tools, Ball Grid Array (BGA) integrated circuit package rework and inspection capability, clean room, and a wire bonder. The BGA rework and inspection tools were especially important because the small form factor requirements for the controller required the use of BGA packages. Optical and X-ray BGA inspection microscopes have already proved valuable in troubleshooting.

The end goal of the Development phase is to design and produce a detector controller capable of running a 1 x 4 assembly of OTAs in a form factor suitable for testing in a laboratory and on a telescope. The goal of the Production phase is to fabricate electronics for four fully functional gigapixel OTA cameras. Production schedule will allow the systems to be produced in a serial fashion.

REQUIREMENTS

1.1. Modes of Operation
The OTA will be operated in a sequence of different modes of clocking and readout to accomplish the overall goal of a corrected science image. The OTA design incorporates specific circuitry that will need to be serviced by the controller electronics to accomplish these modes.

<table>
<thead>
<tr>
<th>Mode Name</th>
<th>Description</th>
<th>OTA operation</th>
<th>Controller Function Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>No integration, no guide</td>
<td>Resets?</td>
<td>Reset OTAs?</td>
</tr>
<tr>
<td>Shutter Control Mode</td>
<td>No integration, no guide</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Guide Star Acquisition mode</td>
<td>~1 sec Integration, ~0.5 sec Readout for ~ 5 guide objects in 5 cells per OTA</td>
<td>Integrate Address cells Clock out</td>
<td>Reset, Integrate timing, Readout, Transport data to Pixelserver computer, Pixelserver computer determines centroids and corresponding clocking patterns for image correction.</td>
</tr>
<tr>
<td>Combined Guide and Integration Mode</td>
<td>Fast clocking and readout of Guide cells</td>
<td>Integrate Address cells Clock out</td>
<td></td>
</tr>
<tr>
<td>Low Noise Readout Mode</td>
<td>(Closed shutter) readout of science image</td>
<td>Integrate Address cells Clock out</td>
<td></td>
</tr>
</tbody>
</table>

The typical sequenced readout of an OTA would be:

Sequenced readout:
- Open Shutter
- Acquire
- ~1 sec integration, readout ~0.5sec
  - Pixelserver determines ~5 guide objects in 5 cells per OTA
- Guide + Integration
  - ~5 guide cell subarray readout at 10-30Hz (<100Hz)
  - Pixelserver centroids and determines guide subarray position
  - Pixelserver also computes OT parallel shift patterns for remaining cell
- Expected Times Nominal 10s of seconds
  - Max ~1000sec
  - Min ~shutter speed/setup
- Apply OT parallel shift clocks (~10usec each)
- Delay ~50msec
- Close shutter and Readout ~2sec

1.1.1. Full Camera operation
- Synchronized clocking to <30nsec.
- Heat dissipation from controller system should not impact seeing.
- System will need active cooling.
- System goal of < 400Watts (On Telescope, per Gigapixel Camera).
- Noise floor 1 LSB, less than 1e-.
- OTA crosstalk must be less than noise floor

1.1.2. OTA Input and Control
• Sequenced readout
• guide rates 10-30Hz
• Nominal guide patch
  o @ 0.3 arcsec/pixel 10 arcsec patch = ~32 X 32 pixels, 10msec/1024 pixels = 9.77 usec/pixel max speed clock+signal condition+ADC+buffer
• Centroid and shift calculation time + Change clock patterns, latency goal = 2msec goal
• Clocking pattern time resolution ~10nsec

1.1.3. OTA Output
• 100K e- well and expected 4e- noise at 1 MHz
• 2e- noise goal at 100 kHz (guiding)
• ADC bit resolution – approx two bits on the noise
  o 100k / 4 = 25K X 2 = 50K resolution wanted
    ▪ 16 bits = 64K (> 14bits)
• Image memory
  o OTA 4096 x 4096 pixels = 16M pixels = 32MBytes (16 bit resolution)
  o 8 x 8 focal plane = 1Gpixel = 2Gbytes (16bit)
• Data buffering and storage
  o Unless data transport is real time, minimum storage is 2Gbytes, 4Gbytes double buffered.
• Memory access speed minimum ~8 to 16Gbits/sec (1 to 2 Gbytes/sec).
• Full 1Gpixel focal plane readout in ~2sec = ~8Gbits/sec
• Signal processing chain
  o 1Gpixel / 64 OTA = 16Mpixels / OTA
  o 16Mpixels / 8 outputs = 2Mpixels/output
  o 2 sec / 2Mpixels = 954nsec/pixel
  o ADC plus settle time ~1usec per output
  o 1Mhz ADC borderline too slow (unless CDS built-in)
• Controller data transport
  o Maximum speed matches Full 1Gpixel focal plane readout in ~2sec = ~8Gbits/sec
  o Minimum speed equal to shortest expected science integration ~10s = 214 Mbits/sec
• Internal (controller) data path >= 8Gbits/sec
• Path to Pixelserver(s) >= 8Gbits/sec

1.1.4. Internal Data Throughput Requirements

<table>
<thead>
<tr>
<th>Stage</th>
<th>Array/ADC Readout</th>
<th>CompactPCI Bus</th>
<th>COTS CPU</th>
<th>1G ethernet</th>
<th>Pixel Processor</th>
<th>Data Storage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Requirement</td>
<td>Min 64MBps Goal 128MBps</td>
<td>Min 64MBps Goal ≥128MBps</td>
<td>Min &gt; 128MBps</td>
<td>Min 64MBps Goal ≥128MBps</td>
<td>Min ≥ 128MBps</td>
<td>Min 64MBps</td>
</tr>
<tr>
<td>Capability</td>
<td>Max 260MBps (5MSPs/ADC x 24)</td>
<td>132MBps theoretical (32 bit) 265MBps (64 bit) *noise &amp; ground isolation</td>
<td>Processor/memory access (read + write)</td>
<td>125MBps theoretical</td>
<td>Processor/memory access (read + write)</td>
<td>Burst ~60MBps Only ~20MBps sustained</td>
</tr>
<tr>
<td>Notes</td>
<td>33.55 Mpixel/sec (~2sec)</td>
<td>Test to confirm</td>
<td>Use dual 1Ge?</td>
<td>133/400/53 Mhz FSB</td>
<td>Duty cycle?</td>
<td></td>
</tr>
</tbody>
</table>
The size and shape of the controller electronics is as much of a driver of the design as the electrical requirements. The short cassegrain depth available on the telescope and the size of the focal plane resulted in a horizontal arrangement with the controllers placed outboard of the mosaic.

The 8 by 8 mosaic focal plane was further broken down into 1 by 4 OTCCD rigid-flex assemblies (see figure). The rigid flex assembly will penetrate the dewar wall and be connectorized for direct attachment to the controller. The ideal size for the chassis would be the width of an individual OTCCD which is ~50mm. The 3U CompactPCI form factor was chosen due to the availability of off the shelf products including standardized connectors that insure electrical, mechanical, thermal, and EMI performance.
ADC TESTING

The proper choice of Analog to Digital Converter (ADC) is critical to achieve the noise, speed and size requirements for the system. After an industry search for an acceptable 16 bit ADC, a series of tests were performed to evaluate the Analog Devices ADC9826, a 16 bit, ~15 to 12.5MSps, 3 channel Imaging Front End. The AD9826 has several non-ideal specifications including a read noise of 3 LSB and integral non-linearity of 16 LSB. Both bench level and focal plane tests were performed with a CCID20 using a small custom test board in a Leach SDSU controller system. Several operational modes were tested and some proved to have performance levels suitable for astronomical CCD instrumentation.

2. Bench Tests

The bench test setup consisted of the custom PCB connected to precision voltage source (actually only specified to 14 bit precision, but adequate for our use) or a Stanford Research Systems arbitrary function generator for a signal input to the test PCB and an Agilent logic analyzer to capture the 9826 digital output. The triggering was DIP switch settable to either self generate out of the CPLD, or synchronize to an external pulse generator. Two test PCBs (=2 AD9826’s) were tested.

We believe testing with the AD9826 inputs directly grounded may not be the best way to check noise performance due to the switched input capacitor input structure of the device (it would be better to drive it with an active source to charge and discharge the input caps). Consequently, the precision voltage source was used to generate a DC voltage. It should be noted that the there was a zero volt offset (zero volts input resulted in a non zero ADU output). The AD9826 internal OFFSET function was checked but not used when taking the noise data in single channel and 3 channel modes. Only relatively fast readout rates were tested (< 20usec). The AD9826 has several operational modes that include sample and hold, internal Correlated Double Sample (CDS), and an internal programmable gain amplifier in the 1,2 and 3 input channel configurations. Only a subset of these modes was tested, but we were able to achieve the datasheet specification for read noise. Further performance levels were reached with a digital average function implemented in the CPLD in which four successive samples were added and then bit shift averaged.

Table 1 Bench Noise Results

<table>
<thead>
<tr>
<th>Test Conditions</th>
<th>300nsec Sample and Hold</th>
<th>100nsec Sample and Hold</th>
<th>100nsec CDS</th>
<th>180nsec CDS with 4 sample digital average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise for DC input</td>
<td>3.667 ADU</td>
<td>3.391 ADU</td>
<td>3.546 ADU</td>
<td>1.690 ADU</td>
</tr>
</tbody>
</table>

2.1. CCID20 testing

The test PCB was placed in one of the 2 normal locations for the SDSU Leach Date937 ADCs and run in a standard system attached to one of several cooled CCID20s. Two primary configurations were used, one that used the entire dual...
slope integrating signal chain on the board and one that only used the front end ac coupling capacitor + input opamp + offset circuit (modified for polarity).

The connection methods used were non-ideal and the data was post processed to remove the 60Hz pickup. When this processing step was used on data obtained in the digital multiple correlated sampling mode, the read noise at 1.2usec pixel rate approached the Datel 937 reference ADC value at a 4usec pixel rate (the Datel 937 4.1e level was nominal for this array and test configuration). Linearity was determined to be ~1% with no evidence of the 16 LSB differential non-linearity specification.

<table>
<thead>
<tr>
<th>Test Conditions</th>
<th>Grounded input Single Channel SHA + Leach front end only + Digital CDS (4-4)/4 samples AD9826</th>
<th>CCD input Bias+dark Single Channel SHA + Leach front end only + Digital CDS (4-4)/4 samples AD9826</th>
<th>CCD Input Bias+dark Standard Leach Datel 937 ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unprocessed Read Noise</td>
<td>2.1ADU</td>
<td>3.5ADU (1.6e/ADU=5.6e) at a 1.2usec rate</td>
<td>4.1ADU (1e/ADU=4.1e) at 4usec rate</td>
</tr>
<tr>
<td>Processed Read Noise</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2.2. Digital Multiple Correlated Sampling (DMCS)

The CPLD was programmed to accumulate a number of pedestal samples, subtract corresponding signal samples and divide the result by the number of sample pairs. The following figure depicts the relative locations of the samples on a typical preamplifier signal. A pixel rate of 1.2usec was tested with at multiple sample rate of 120nsec. Although the test performance did not meet the PanSTARRS final goal for ADC read noise, the promising DMCS mode data convinced the team to proceed to the prototype phase using the AD9826.
The schedule for the prototype design is driven by MIT/LL Lot#1 production of the OTCCDs. It is intended to allow full testing of OTAs, but will not support full high-speed data transport. Four 100BT interfaces (with optional fiber conversion) were deemed adequate for testing. Early tests indicate that a sustained ~5 Mbytes/sec/link = 20MBytes/sec should be possible. The prototype consist of 5 major components:

- Data acquisition (DAQ3U) PCBs that handle the clocking, pixel processing and data transport.
- Preamplifier and bias buffer PCBs (PREAMP3U) with 8 instrumentation amplifier channels each.
- A single JTAG programming PCB that configures the FPGAs on the DAQ3Us.
- A Pixelserver that controls the system, processes and stores data.
- A 100BT switch for the ethernet links.
The DAQ3U prototype design resulted in a 16 layer controlled impedance PCB with the following functionality:

- Xilinx Virtex2pro V2P7, 672 ball BGA FPGA
- 300MHz PowerPC405 hardcore
- LINUX OS
- 100BT Ethernet communications interface
- DDR SDRAM SODIMM
  - SSTL2 100MHz interface
- 12 Analog Devices ADC9826 Analog to Digital Converters
  - 1 to 3 channels per ADC
  - 12.5MSPS in single channel mode
- 32 channel, 14 bit Analog Devices AD5532 DACs
- LVDS external clock+strobe

Preparations for a preliminary test with a CCID20 are underway to qualify the performance of the controller. Testing of the first MITLL production lot will follow that. We intended to incorporate
POST PROTOTYPE PHASE

The final configuration of IOTA will include the addition one data aggregation and transport board for 4 OTAs. The plan is to redesign the PREAMP and DAQ3U prototypes to handle 16 array channels each. A high-speed data path from each DAQ3U (using the Xilinx Multi-gigabit Transceiver serial interface) will connect to the data aggregation board. This board is targeted to have a 1 Gigabit ethernet interface with full TCP/IP support. We will be investigating using Transmission Offload Engines (TOEs), Network Processor Units (NPUs) and the possible use of the iSCSI protocol for data storage on a Storage Area Network (SAN) or Network Attached Storage (NAS).

![Full Focal Plane Configuration](image)

Preliminary data storage tests on low cost examples of the Pixelserver have been promising. Previous array controller designs have had the bottlenecks in the data transport and data storage portions of the system. Simple testing with commercial PC’s passing data over a 1 G ethernet switch, using the nsf3 protocol, at>50 CPU utilization was 56Mbytes/sec to disk. Test conditions were:

* Ethernet NIC: Intel e1000 ID 0x100e
* Ethernet MTU: 1500
* Ethernet Switch: 1 Ge Cicso
* Processor: Single 2.4 GHz P4 with hyperthreading enabled
* Kernel: Vanilla 2.4.26
## Data Storage and Transport Comparison

<table>
<thead>
<tr>
<th>System</th>
<th>Array/ADC Readout</th>
<th>Fiber Interface</th>
<th>Pixel Input</th>
<th>CDS &amp; Coadd</th>
<th>Transport to Data Storage</th>
<th>Data Storage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Redline/Redstar2</td>
<td>64MBps max</td>
<td>200MBps</td>
<td>320MBps</td>
<td>~40MBps</td>
<td>12-23 MBps actual</td>
<td>&lt;5MBps</td>
</tr>
<tr>
<td></td>
<td>multiplexed across backplane</td>
<td>custom Fiber Channel X2</td>
<td>Ixthos DSP interface X2</td>
<td>~160MBps limit</td>
<td>VME64</td>
<td>Themis USPARCII SCSI 2</td>
</tr>
<tr>
<td>Redstar3</td>
<td>64MBps max</td>
<td>~247MBps</td>
<td>&lt;267MBps</td>
<td>40-60MBps</td>
<td>20MBps Internal RAID</td>
<td>20-40MBps RAID SAN optional</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single Systran SL240</td>
<td>(89-178 MBps typ)</td>
<td>&lt;1.06GBps limit</td>
<td>Or &lt;100MBps</td>
<td></td>
</tr>
<tr>
<td>IOTA 1 X 4 OTA config</td>
<td>384MBps max</td>
<td>~100MBps theoretical 1G ethernet</td>
<td>&lt;534MBps PCI 64bit,66MHz</td>
<td>Pentium and front side bus limited</td>
<td>~100MBps theoretical 1G ethernet</td>
<td>~56MBps tested RAID SAN optional</td>
</tr>
</tbody>
</table>

### ACKNOWLEDGEMENTS

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### REFERENCES

1. Barry Burke et al., elsewhere in these Proceedings.